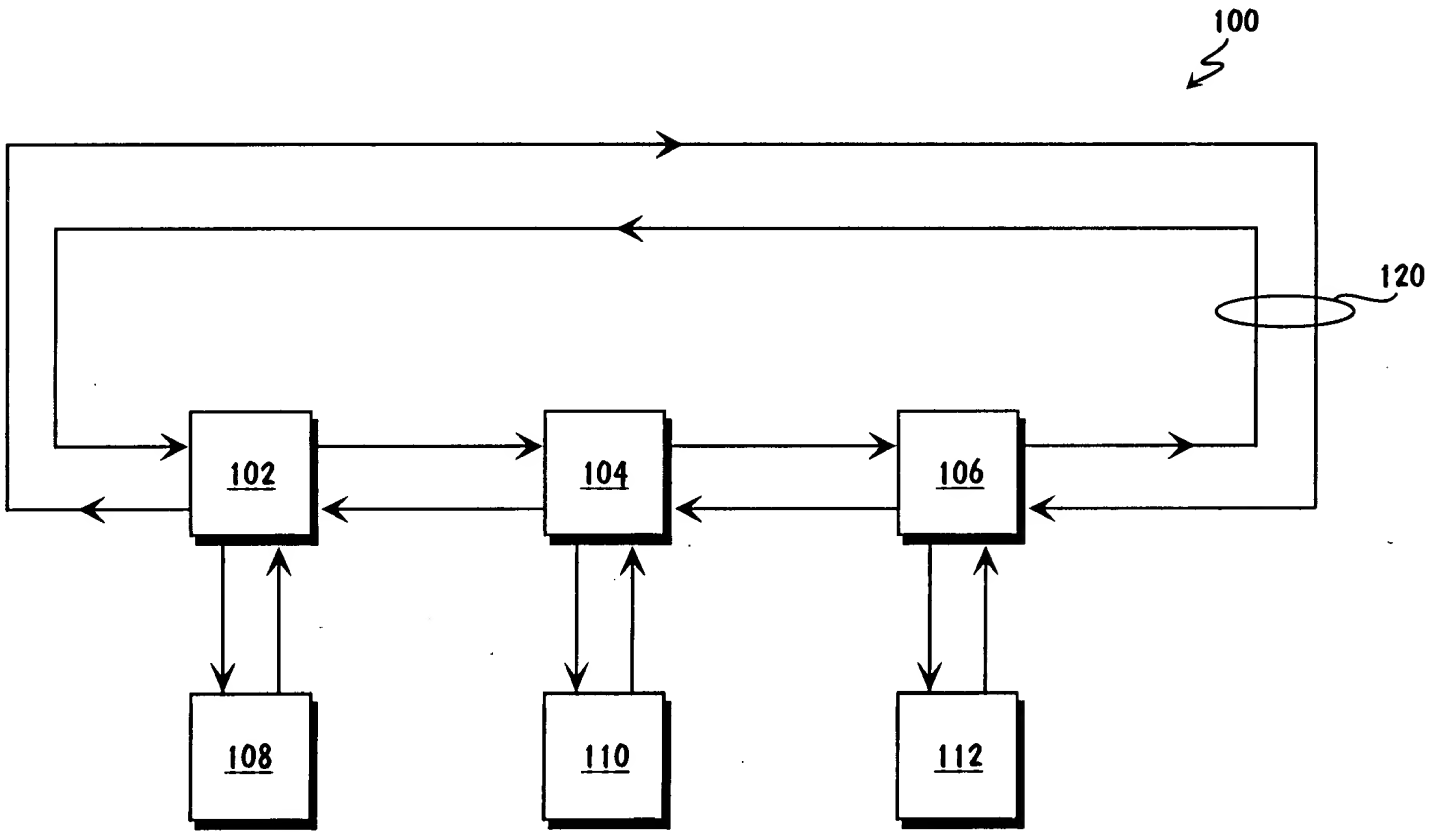

FIG. 1 (PRIOR ART)

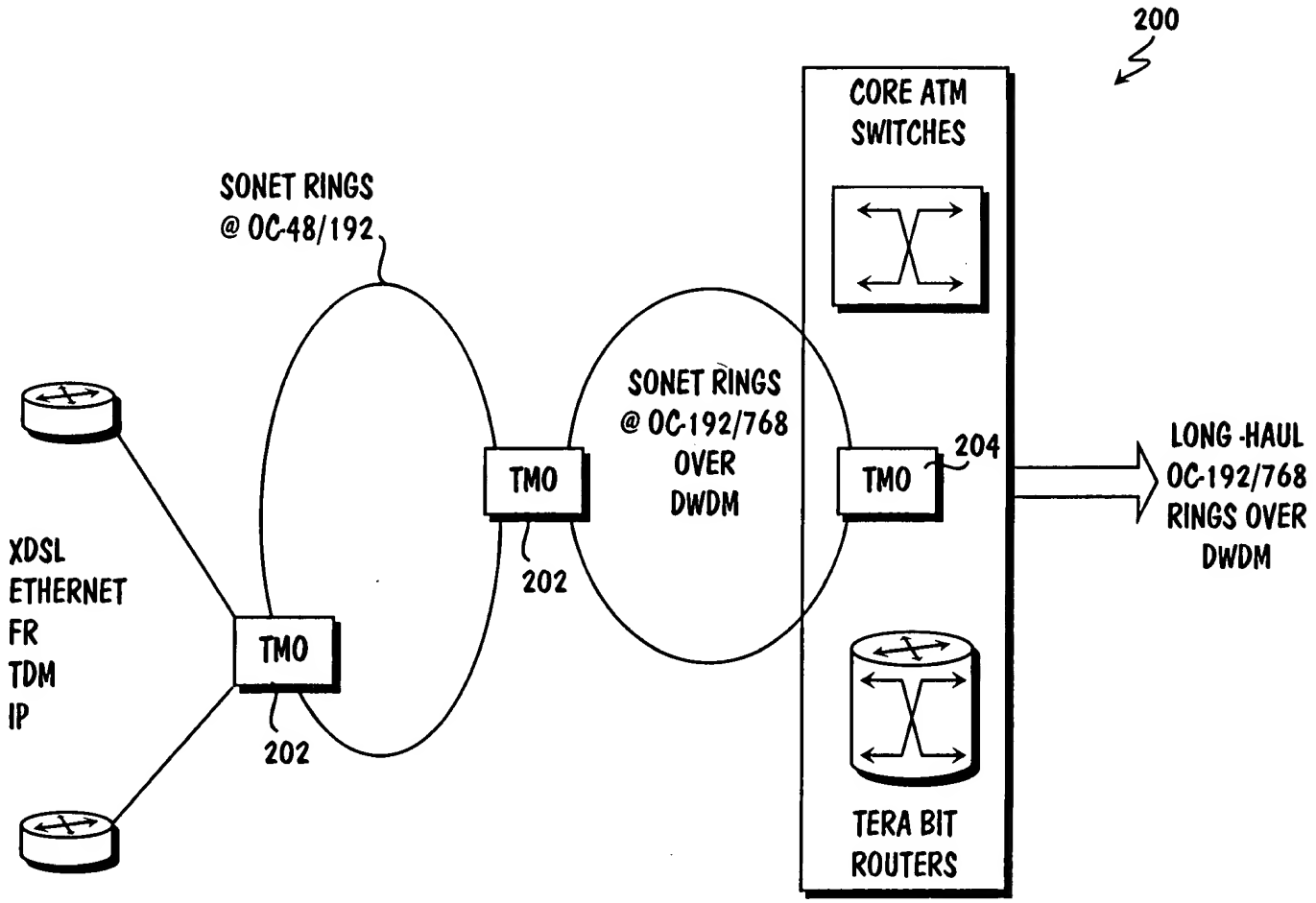

FIG. 2

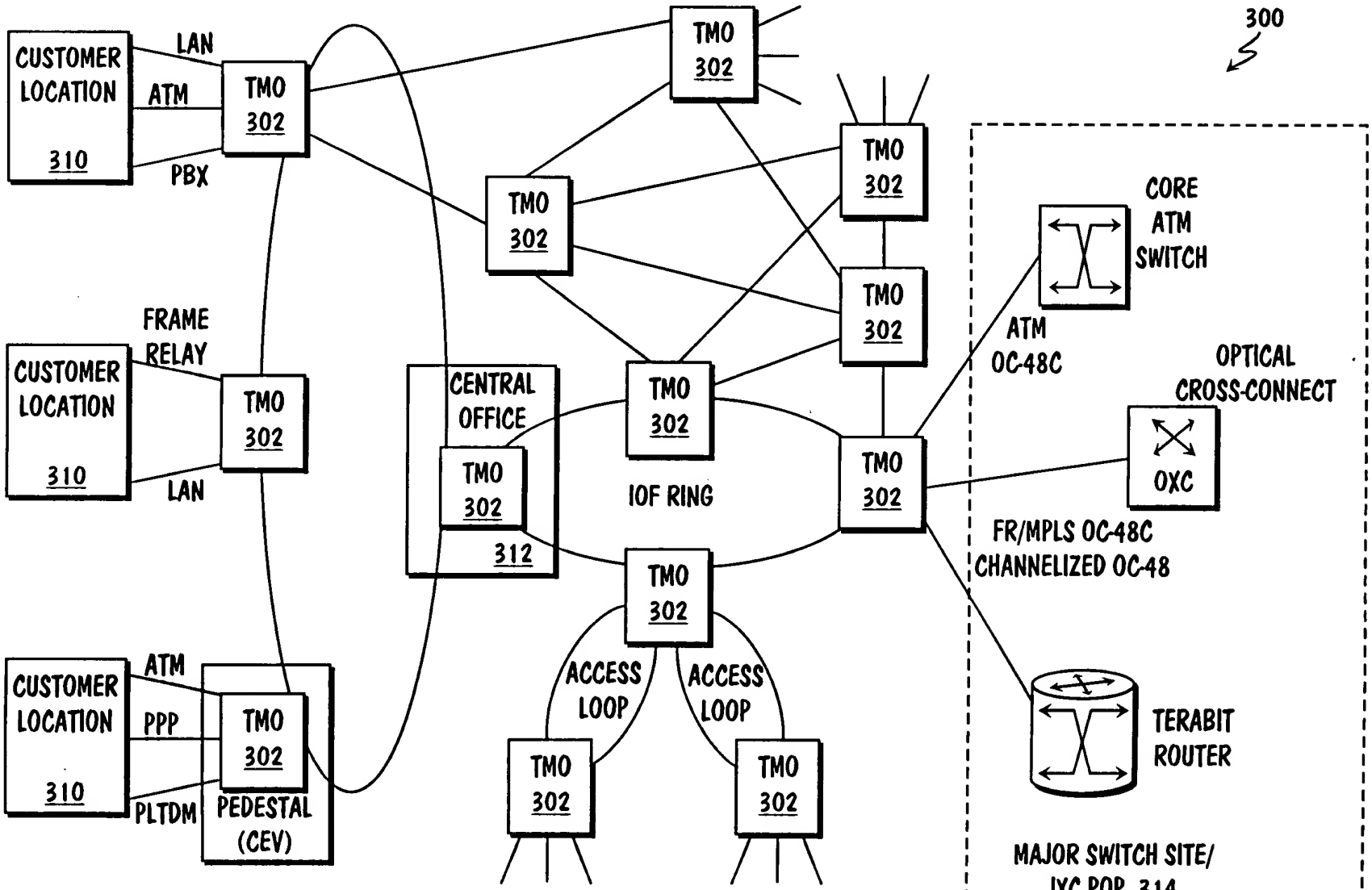

FIG. 3

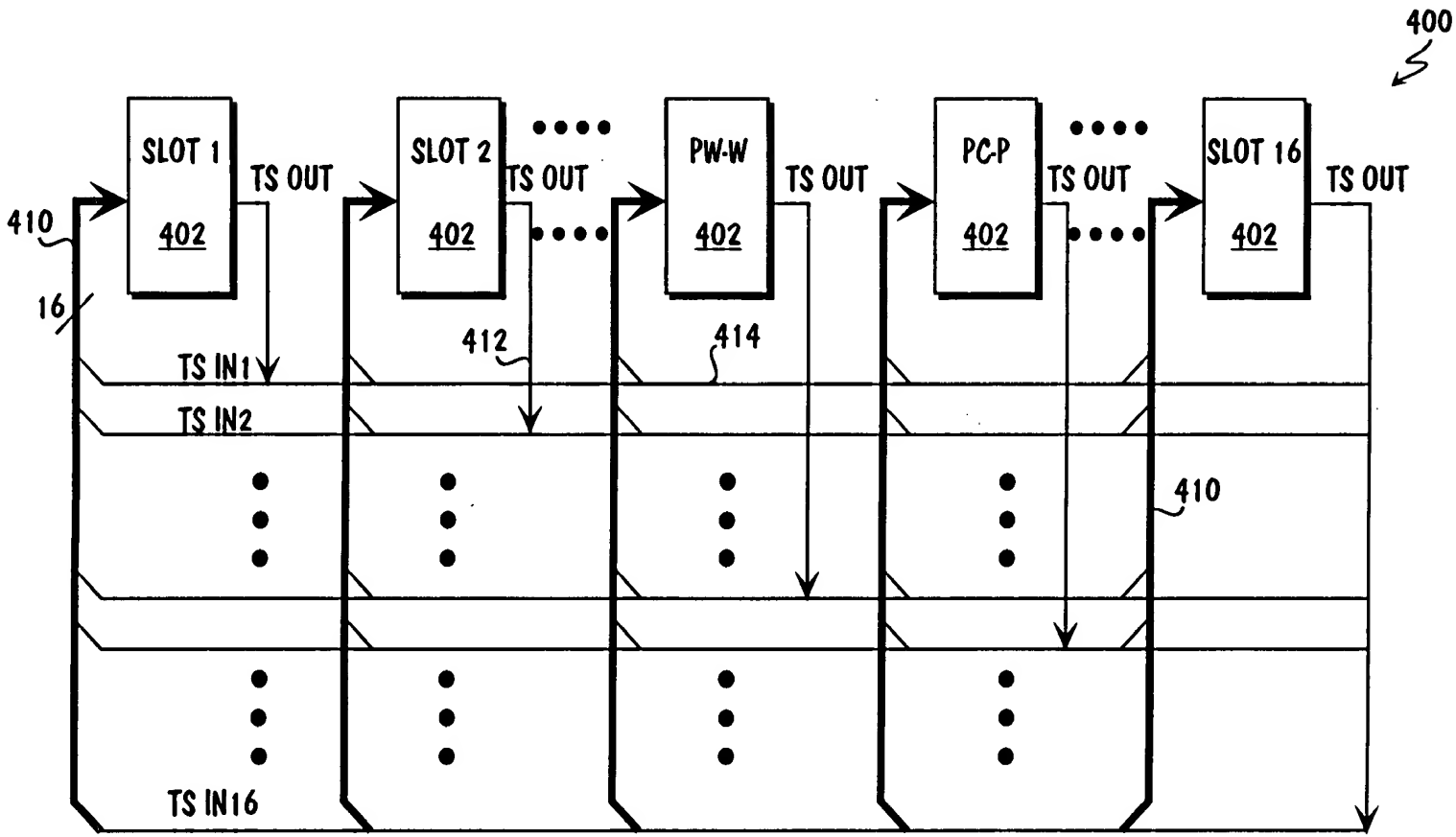
400
SLOT 1
402
TS OUT
SLOT 2
402
TS OUT
PW-W
402
TS OUT
PC-P
402
TS OUT
SLOT 16
402
TS OUT
410
16
412
414
TS IN1
TS IN2
410
TS IN16

FIG. 4

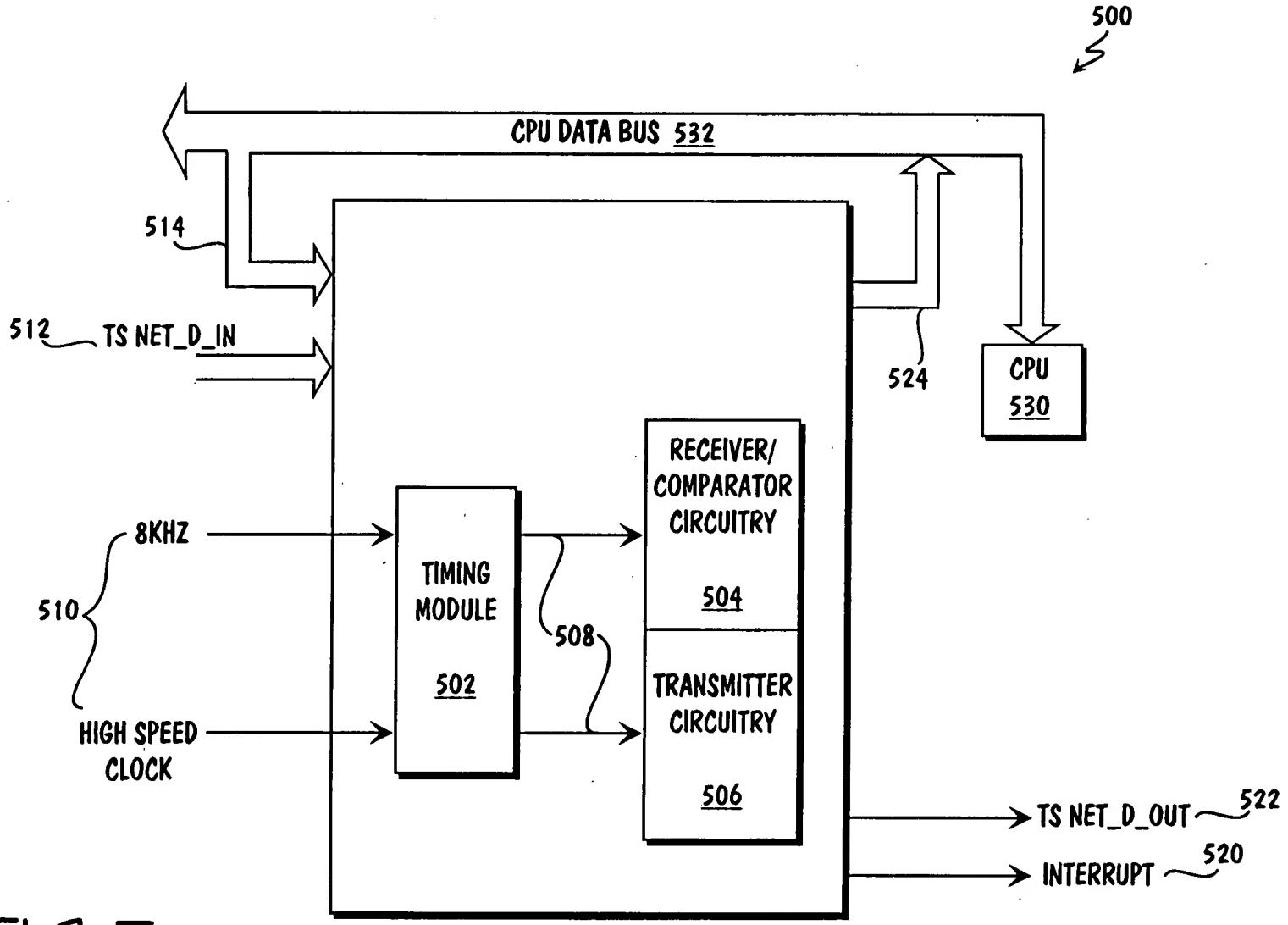
500
CPU DATA BUS 532
514
512
TS NET_D_IN
524
CPU
530
RECEIVER/
COMPARATOR
CIRCUITRY
504
8KHZ
510
TIMING
MODULE
502
508
HIGH SPEED
CLOCK
TRANSMITTER
CIRCUITRY
506
TS NET_D_OUT
522
INTERRUPT
520

FIG. 5

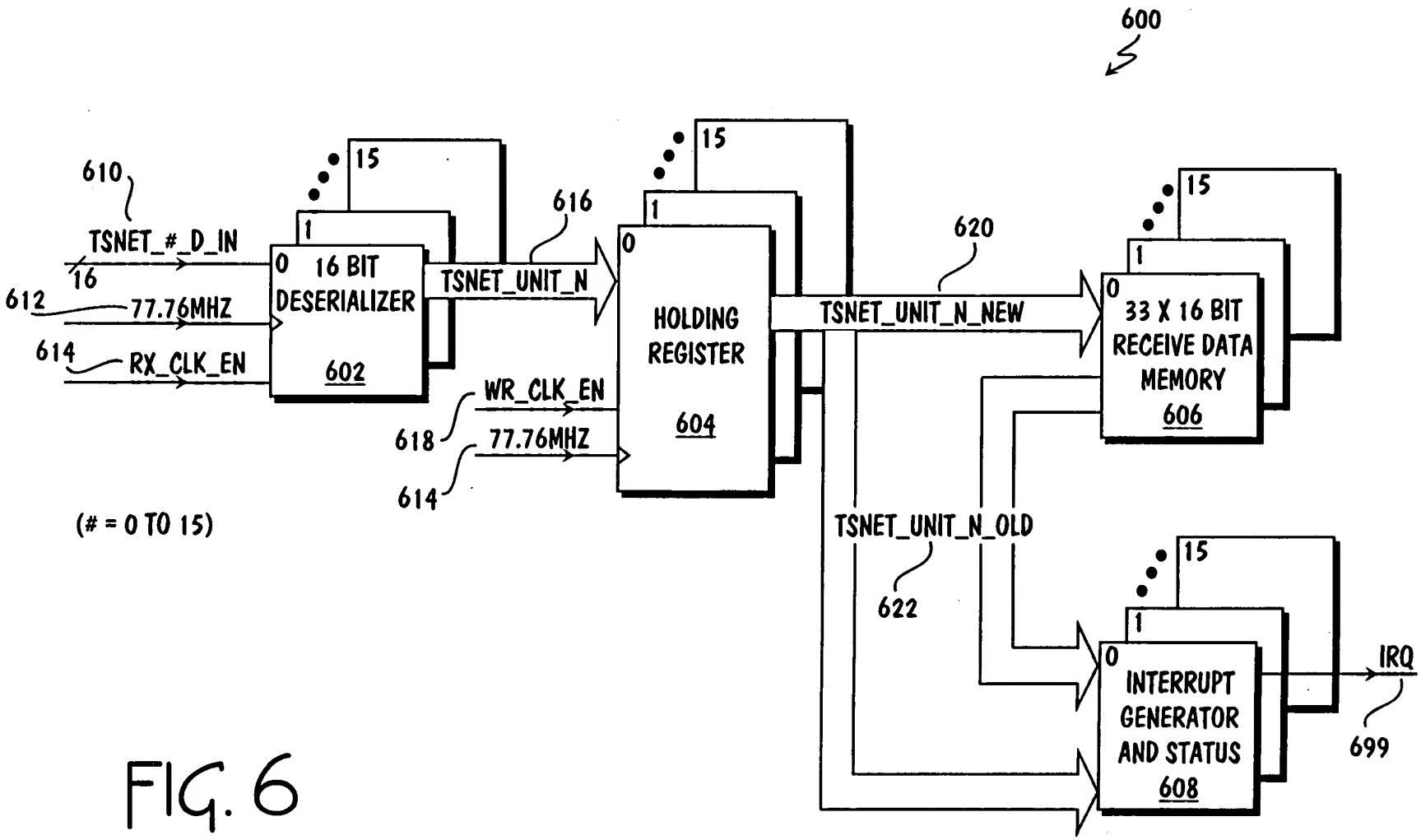
600
610
TSNET_#_D_IN
16
612
77.76MHZ
614
RX_CLK_EN
15
1
0
16 BIT
DESERIALIZER
602
616
TSNET_UNIT_N
15
1
0
HOLDING
REGISTER
604
WR_CLK_EN
618
77.76MHZ
614
620
TSNET_UNIT_N_NEW
15
1
0
33 X 16 BIT
RECEIVE DATA
MEMORY
606
(# = 0 TO 15)
TSNET_UNIT_N_OLD
622
15
1
0
INTERRUPT
GENERATOR
AND STATUS
608
IRQ
699

FIG. 6

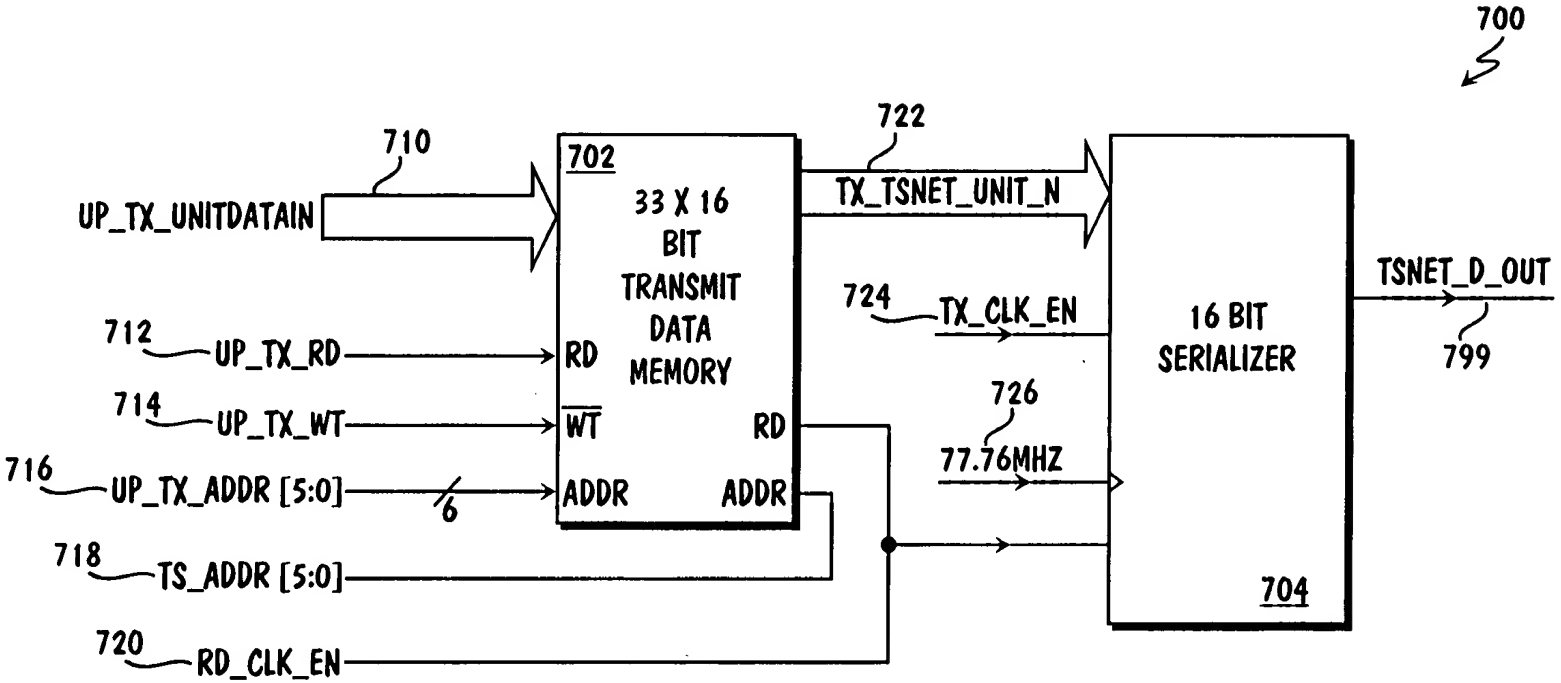
700
710
UP_TX_UNITDATAIN
702
33 X 16
BIT
TRANSMIT
DATA
MEMORY
722
TX_TSNET_UNIT_N
724
TX_CLK_EN
726
77.76MHZ
16 BIT
SERIALIZER
704
TSNET_D_OUT
799
712
UP_TX_RD
RD
714
UP_TX_WT
WT
RD
716
UP_TX_ADDR [5:0]
6
ADDR
ADDR
718
TS_ADDR [5:0]
720
RD_CLK_EN

FIG. 7

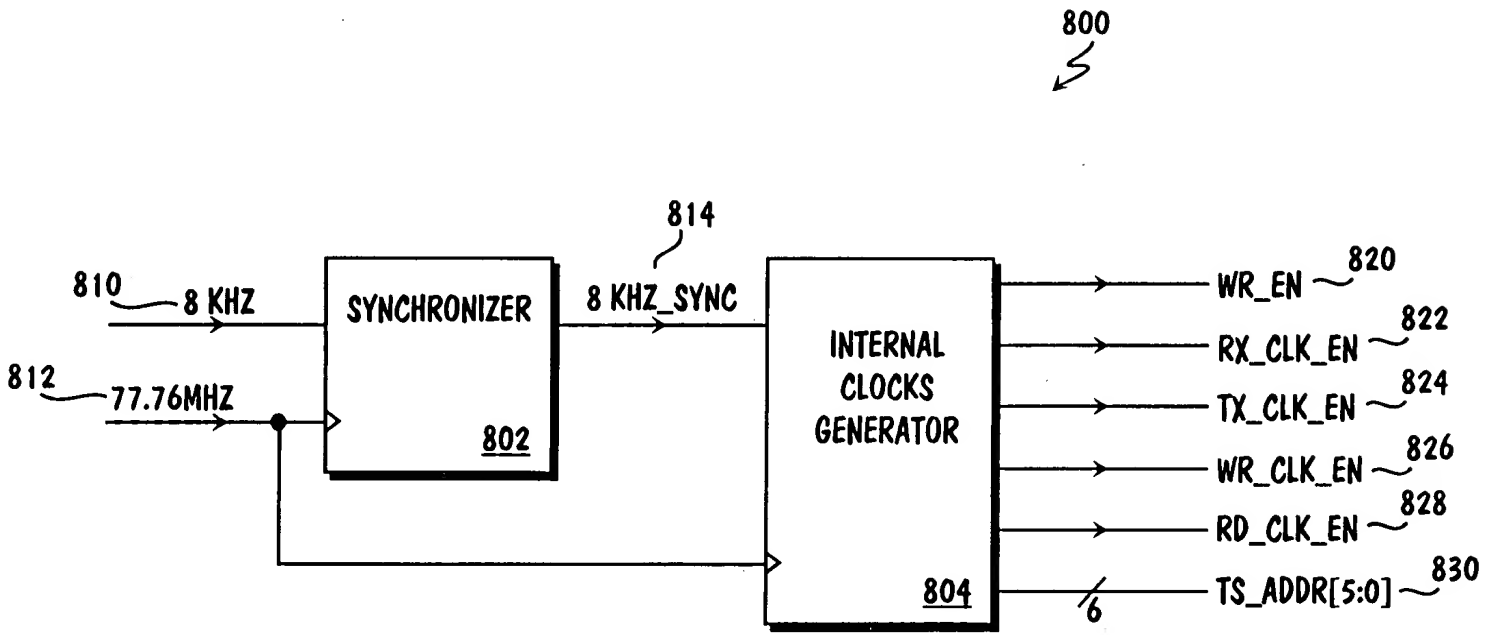
800
814
810
8 KHZ
812
77.76MHZ
SYNCHRONIZER
802
8 KHZ_SYNC
INTERNAL
CLOCKS
GENERATOR
804
WR_EN
820
RX_CLK_EN
822
TX_CLK_EN
824
WR_CLK_EN
826
RD_CLK_EN
828
6
TS_ADDR[5:0]
830

FIG. 8

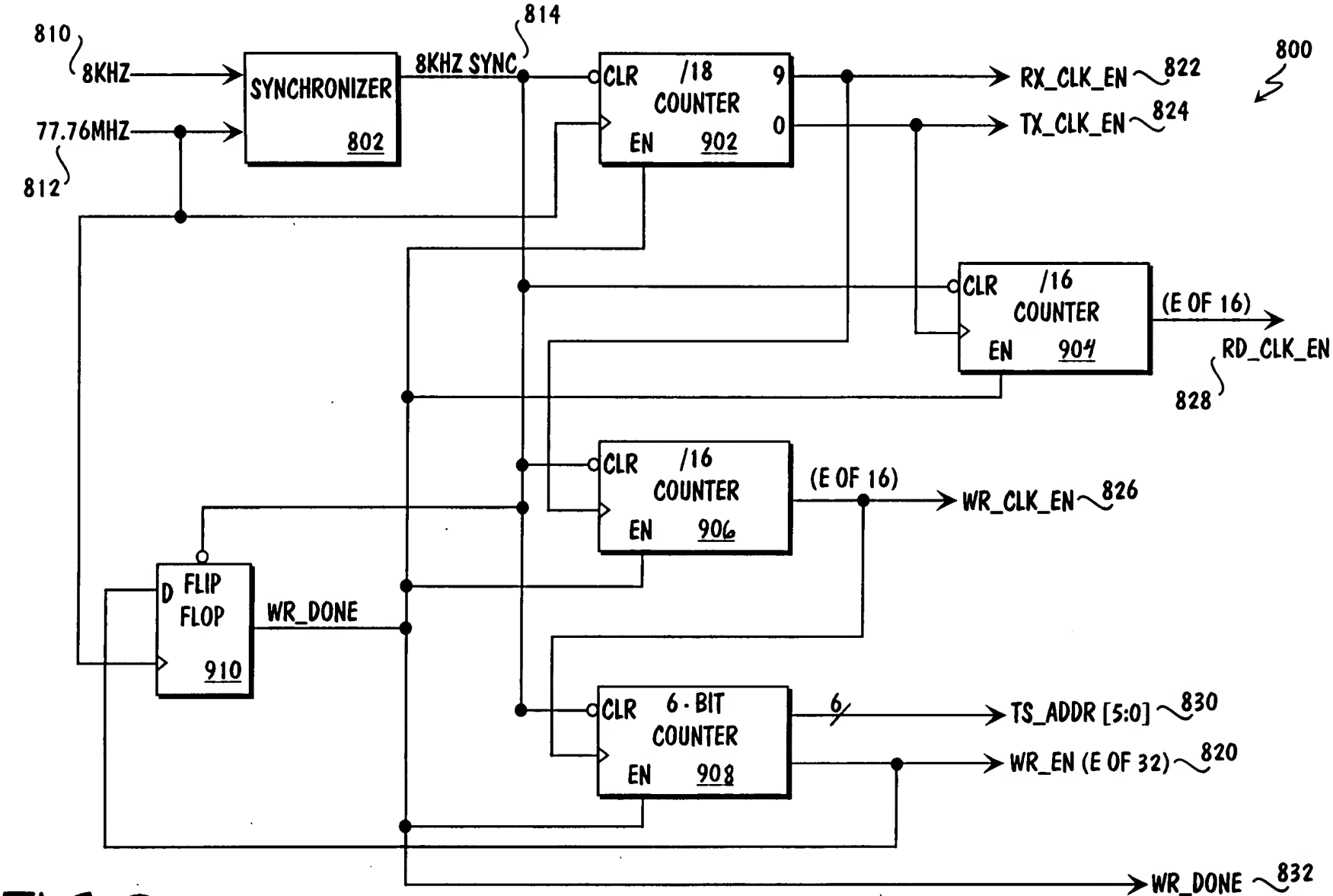
810
8KHZ
77.76MHZ
812
SYNCHRONIZER
802
8KHZ SYNC
814
CLR /18 COUNTER EN 902
9
0
RX_CLK_EN 822
TX_CLK_EN 824
800
CLR /16 COUNTER EN 904
(E OF 16)
RD_CLK_EN
828
CLR /16 COUNTER EN 906
(E OF 16)
WR_CLK_EN 826
D FLIP FLOP 910
WR_DONE
CLR 6-BIT COUNTER EN 908
6
TS_ADDR [5:0] 830
WR_EN (E OF 32) 820
WR_DONE 832

FIG. 9

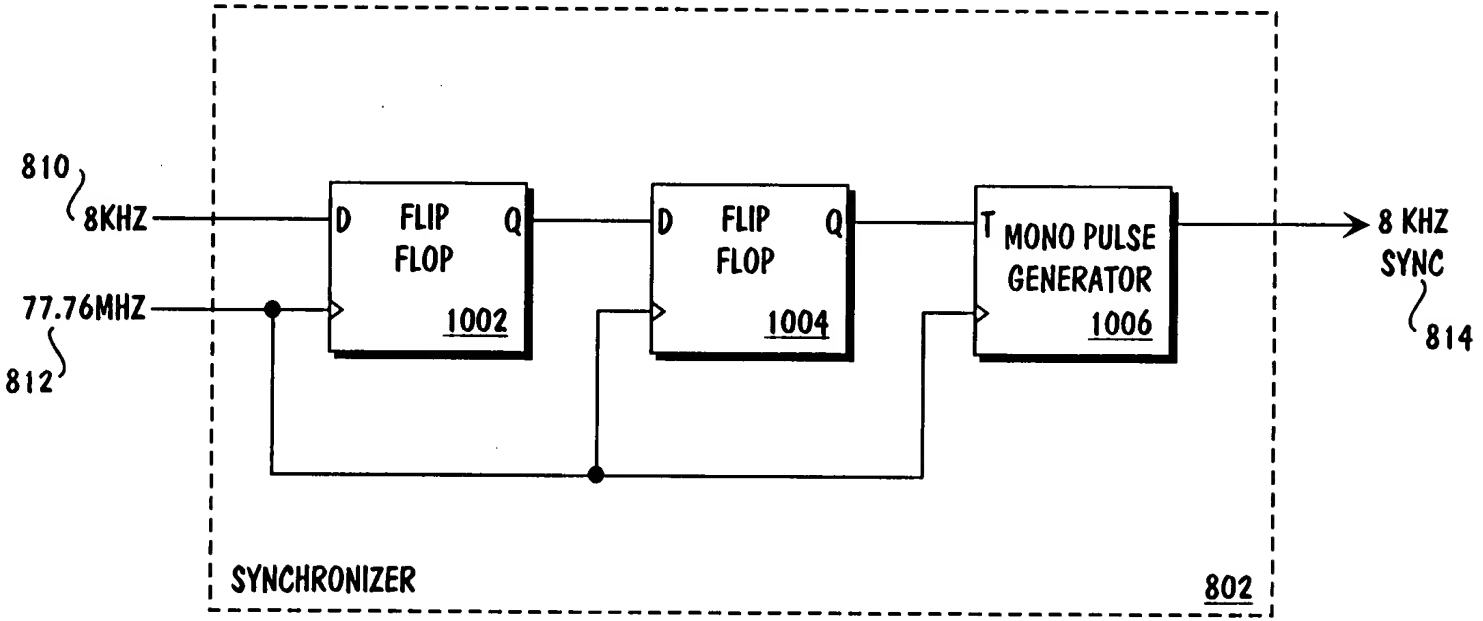

FIG. 10

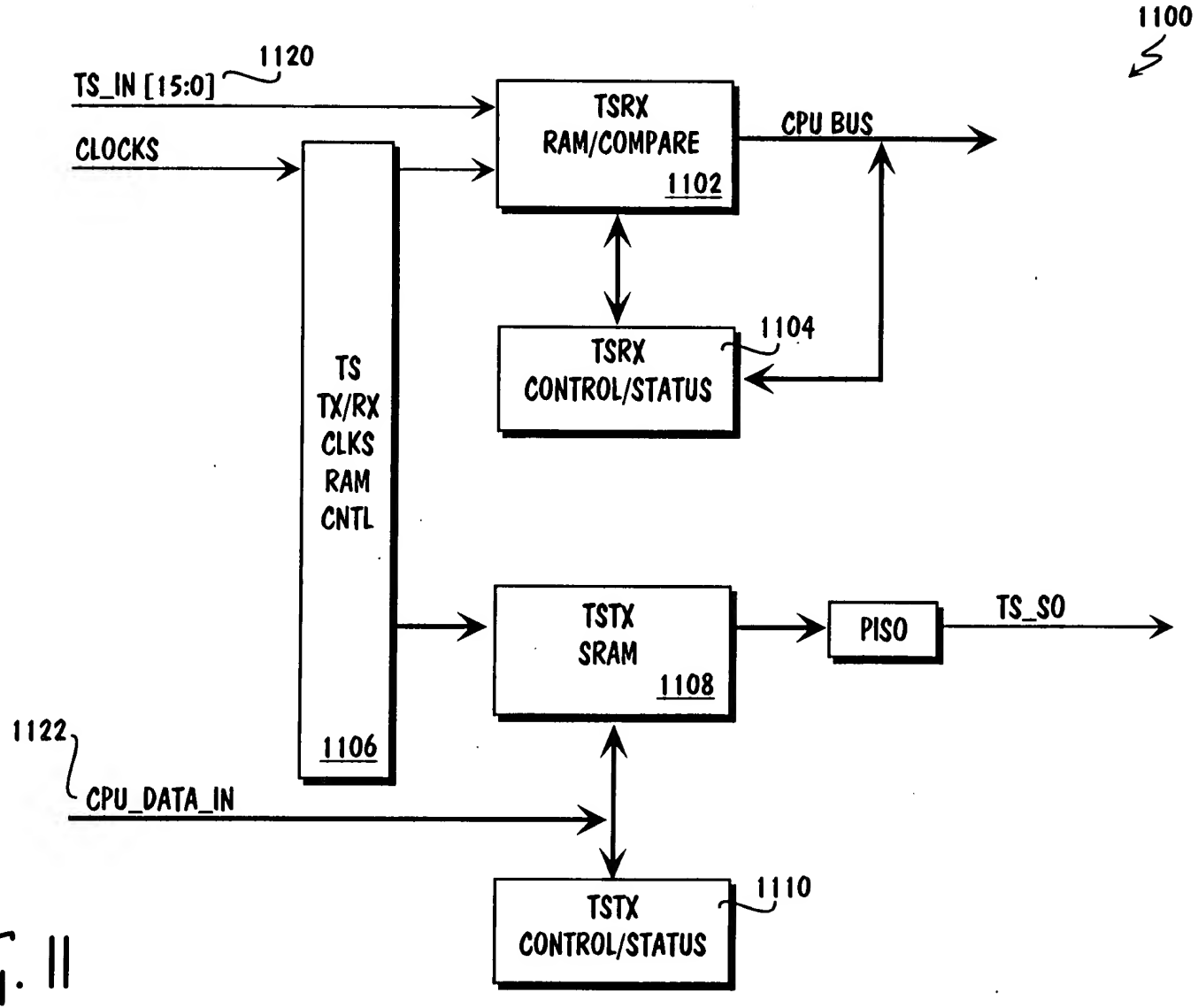
1100
1120
TS_IN [15:0]
CLOCKS
TSRX
RAM/COMPARE
1102
CPU BUS
TSRX
CONTROL/STATUS
1104
TS
TX/RX
CLKS
RAM
CNTL
1106
TSTX
SRAM
1108
PISO
TS_SO
1122
CPU_DATA_IN
TSTX
CONTROL/STATUS
1110

FIG. 11

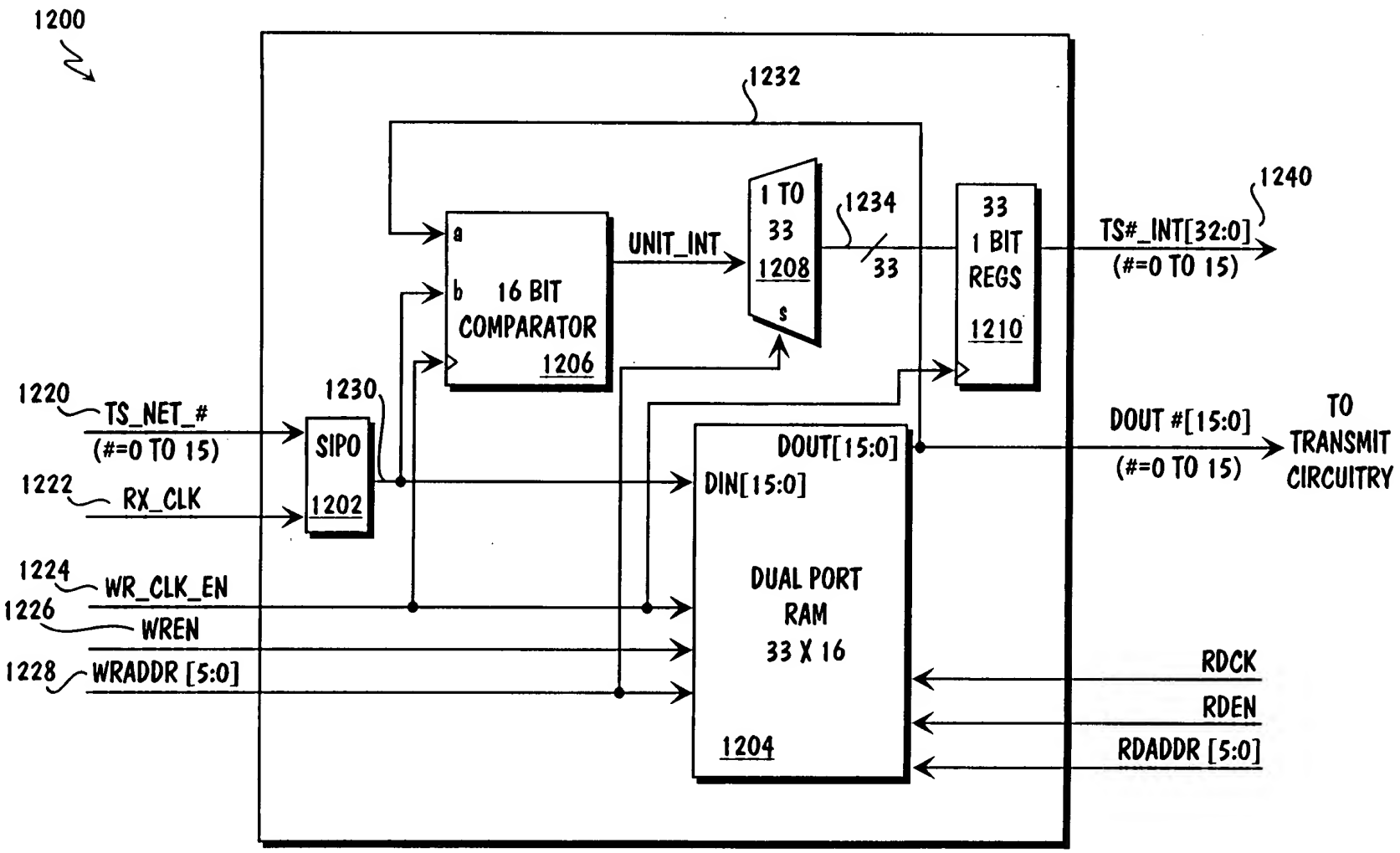
1200
1232
1240
1234
1 TO
33
1208
33
1 BIT
REGS
1210
TS#_INT[32:0]
(#=0 TO 15)
a
b
16 BIT
COMPARATOR
1206
UNIT_INT
1220
TS_NET_#
(#=0 TO 15)
1230
SIPO
1202
1222
RX_CLK
DOUT[15:0]
DIN[15:0]
DUAL PORT
RAM
33 X 16
1204
DOUT #[15:0]
(#=0 TO 15)
TO
TRANSMIT
CIRCUITRY
1224
WR_CLK_EN
1226
WREN
1228
WRADDR [5:0]
RDCK
RDEN
RDADDR [5:0]

FIG. 12A

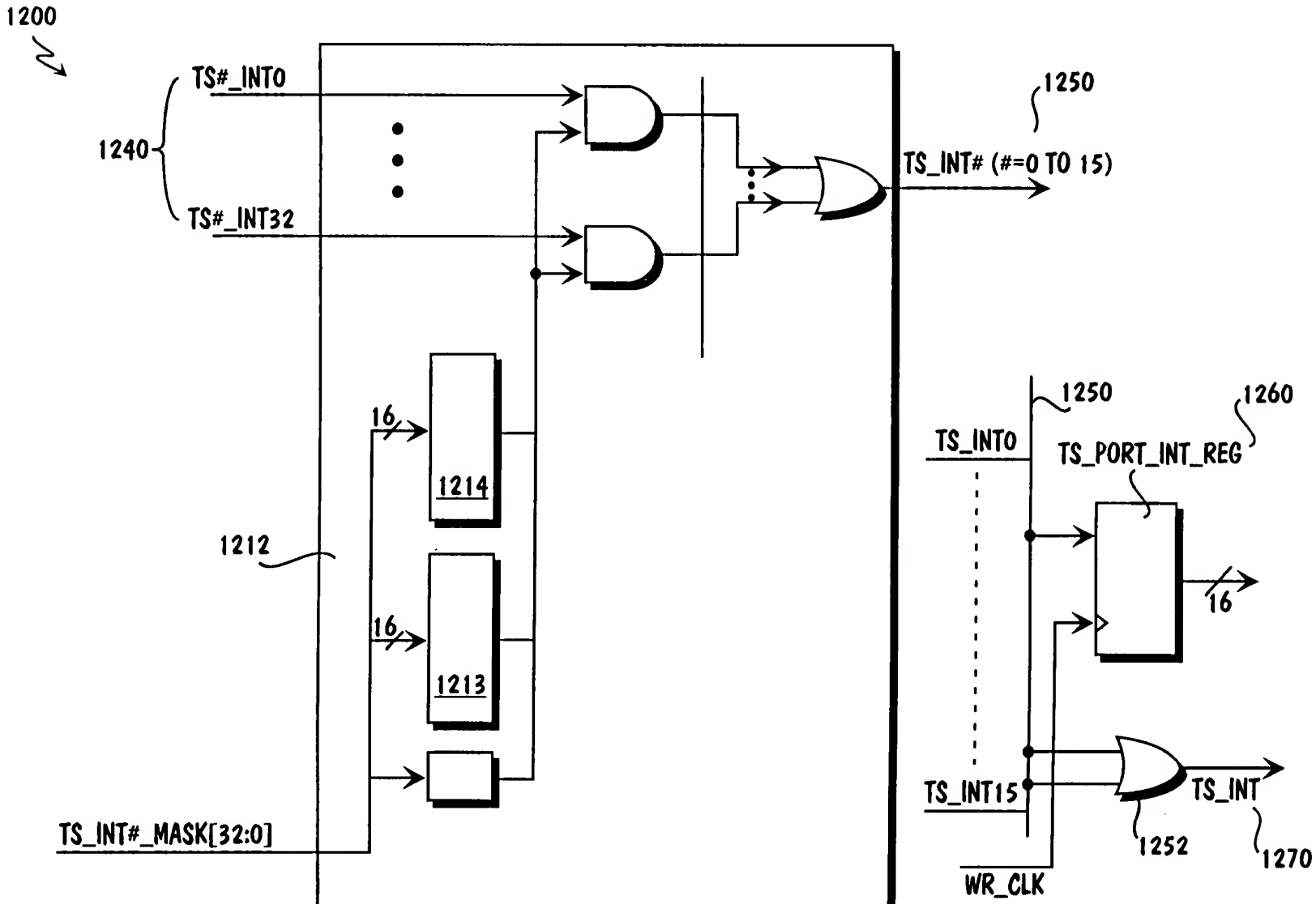
1200
TS#_INT0
1240
TS#_INT32
1250
TS_INT# (#=0 TO 15)
16
1214
1212
16
1213
TS_INT#_MASK[32:0]
1250
1260
TS_INT0
TS_PORT_INT_REG
16
TS_INT15
TS_INT
1252
1270
WR_CLK

FIG. 12B

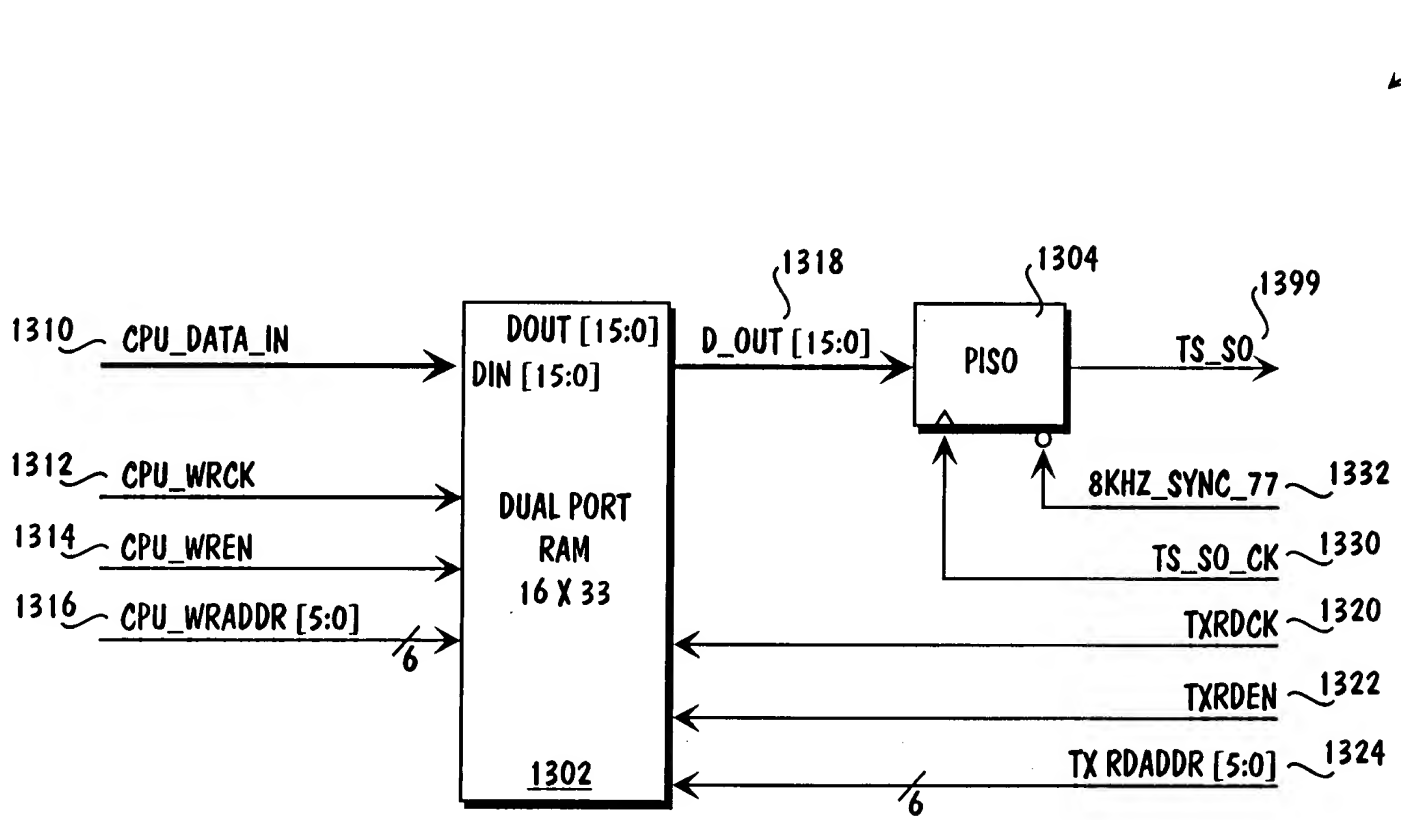
1300
1310
CPU_DATA_IN
1312
CPU_WRCK
1314
CPU_WREN
1316
CPU_WRADDR [5:0]
6
DOUT [15:0]
DIN [15:0]
DUAL PORT
RAM
16 X 33
1302
1318
D_OUT [15:0]
1304
PISO
1399
TS_SO
8KHZ_SYNC_77
1332
TS_SO_CK
1330
TXRDCK
1320
TXRDEN
1322
TX RDADDR [5:0]
1324
6

FIG. 13

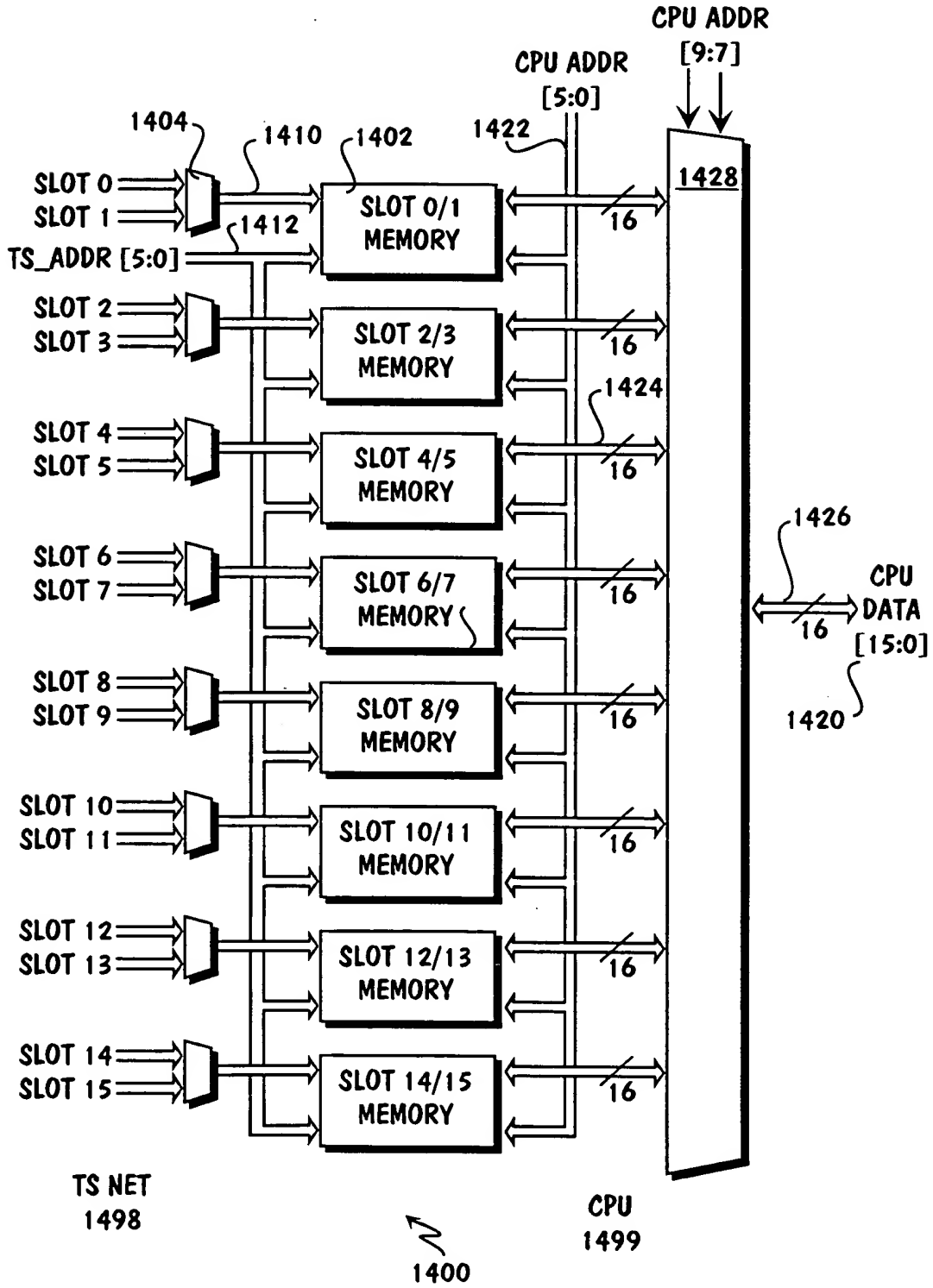

FIG. 14

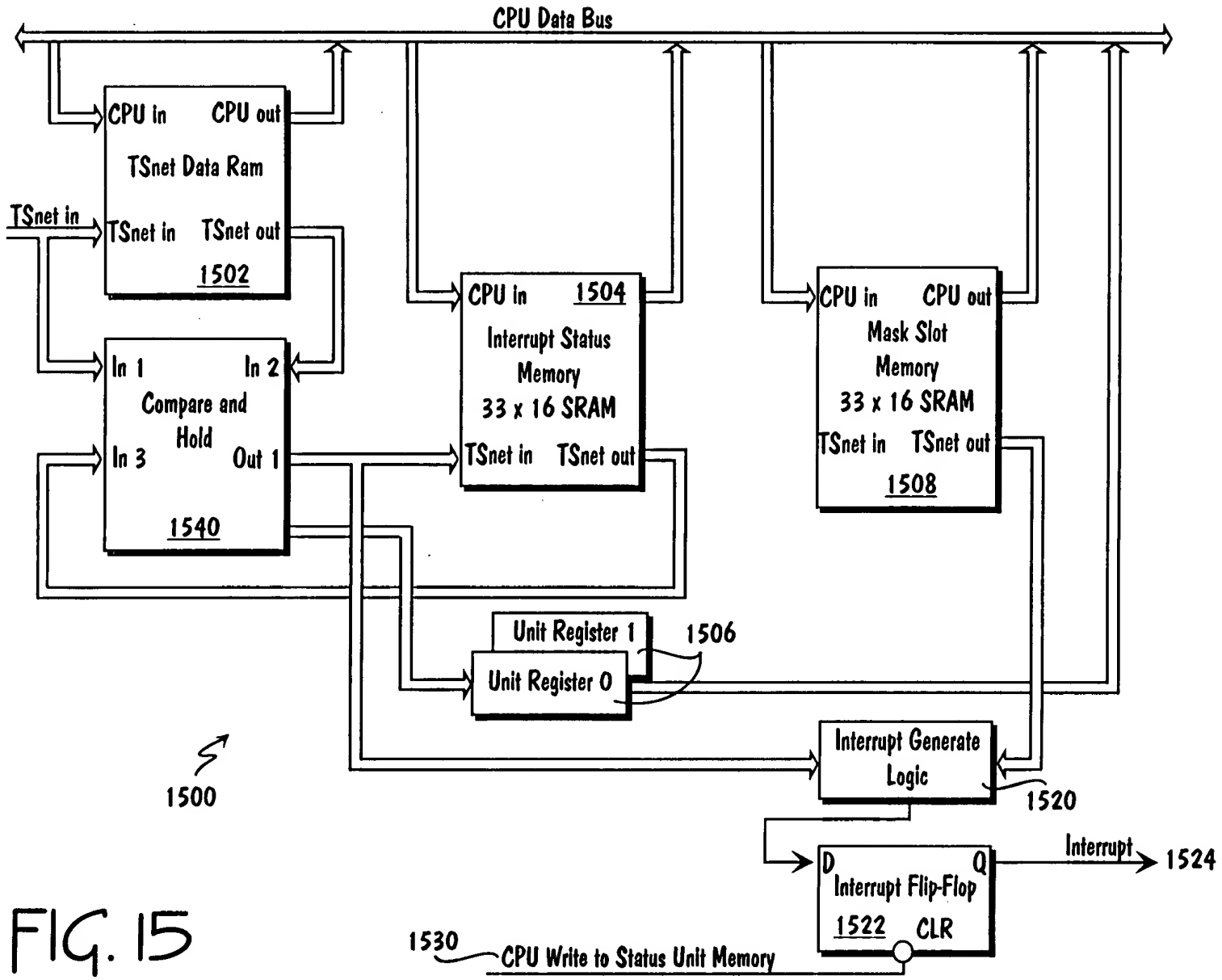
CPU Data Bus
CPU in
CPU out
TSnet Data Ram
TSnet in
TSnet in
TSnet out
1502
CPU in
1504
Interrupt Status
Memory
33 x 16 SRAM
TSnet in
TSnet out
CPU in
CPU out
Mask Slot
Memory
33 x 16 SRAM
TSnet in
TSnet out
1508
In 1
In 2
Compare and
Hold
In 3
Out 1
1540
Unit Register 1
1506
Unit Register 0
1500
Interrupt Generate
Logic
1520
D
Q
Interrupt Flip-Flop
1522
CLR
Interrupt
1524
1530
CPU Write to Status Unit Memory

FIG. 15

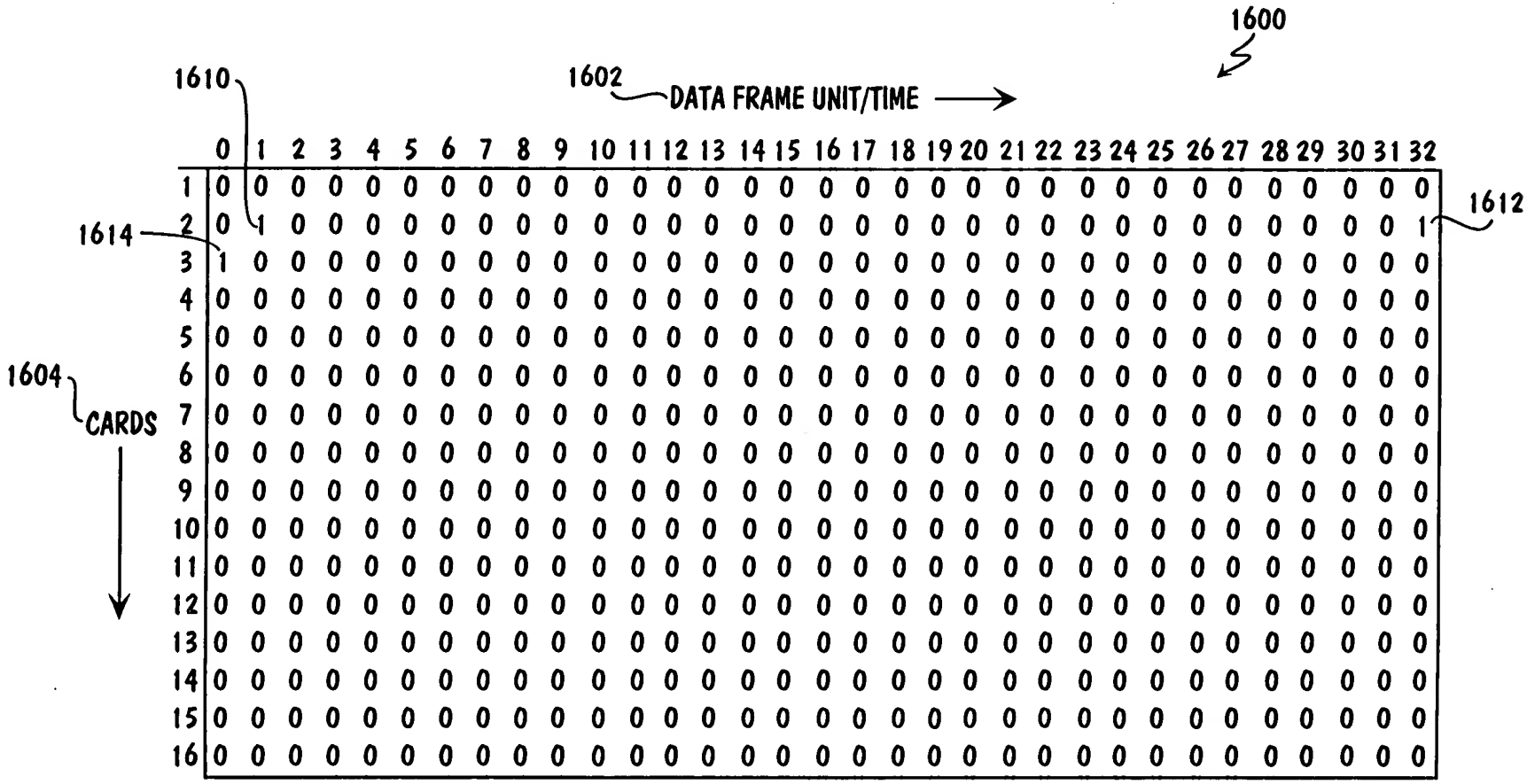

FIG. 16

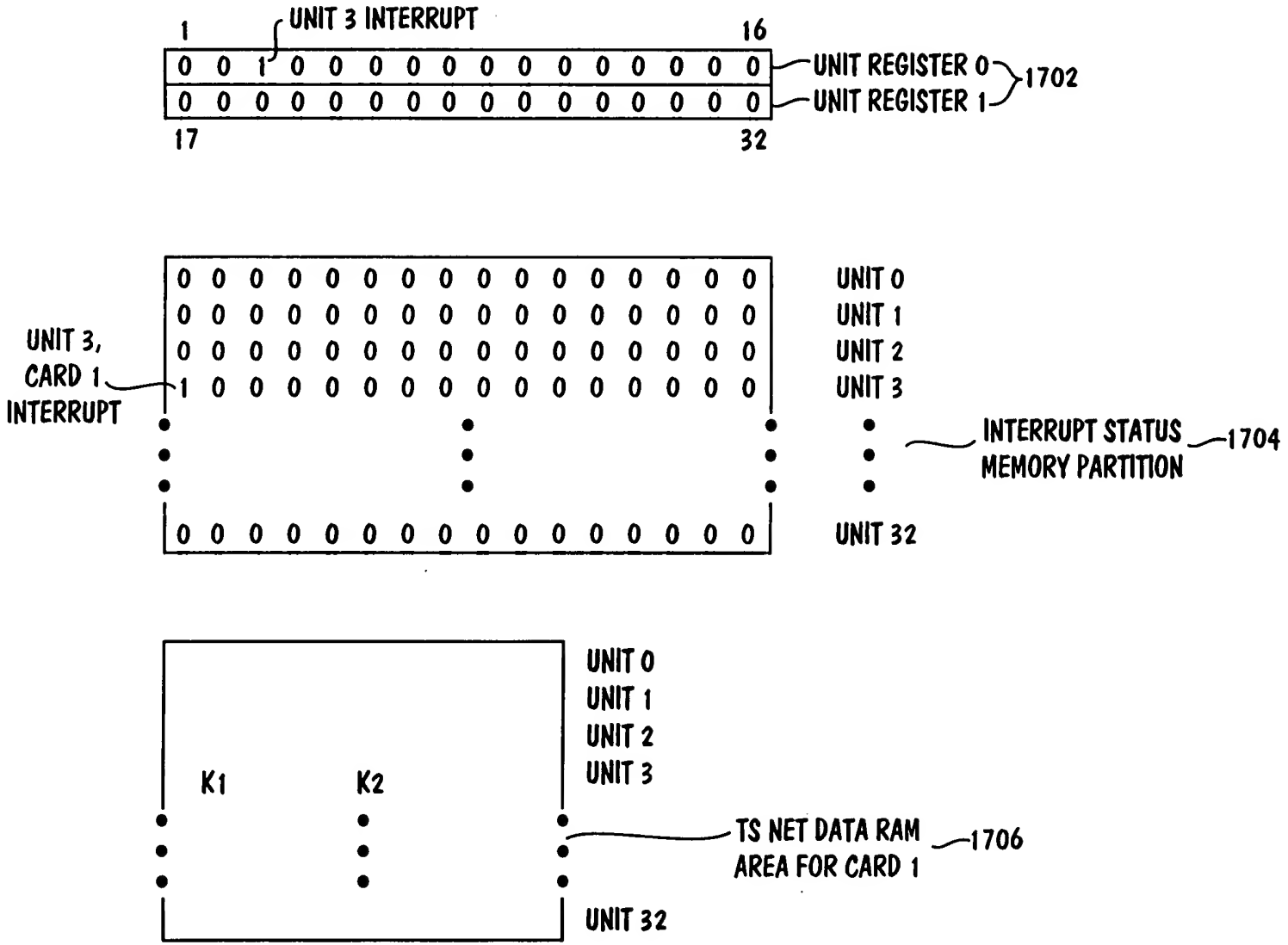
1
UNIT 3 INTERRUPT
16
0 0 1 0 0 0 0 0 0 0 0 0 0 0 0 0
UNIT REGISTER 0
0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
UNIT REGISTER 1
1702
17
32
0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
UNIT 0
0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
UNIT 1
0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
UNIT 2
UNIT 3,
CARD 1
INTERRUPT
1 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
UNIT 3
INTERRUPT STATUS
MEMORY PARTITION
1704
0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
UNIT 32
UNIT 0
UNIT 1
UNIT 2
UNIT 3
K1
K2
TS NET DATA RAM
AREA FOR CARD 1
1706
UNIT 32

FIG. 17

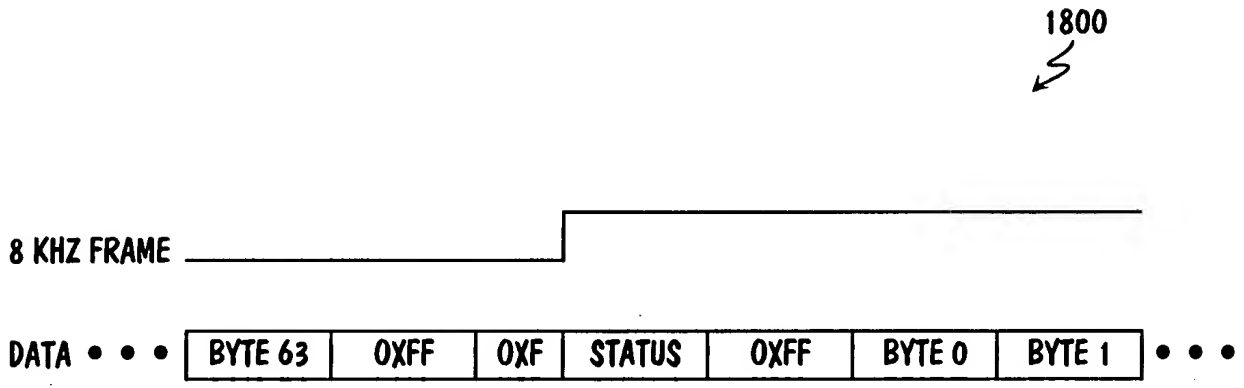
1800
8 KHZ FRAME
DATA
BYTE 63
0XFF
0XF
STATUS
0XFF
BYTE 0
BYTE 1

FIG. 18

BIT	7 (MSB)	6	5	4	3	2	1	0 (LSB)
FUNCTION	BRDSTS1	BRDSTS0	1	1	1	1	1	1

STSB1	STSB0	INTERPRETATION
0	0	PRESENT & FAILED (OR NOT BOOTED)
0	1	PRESENT & INACTIVE
1	0	PRESENT & ACTIVE
1	1	NOT PRESENT

FIG. 19

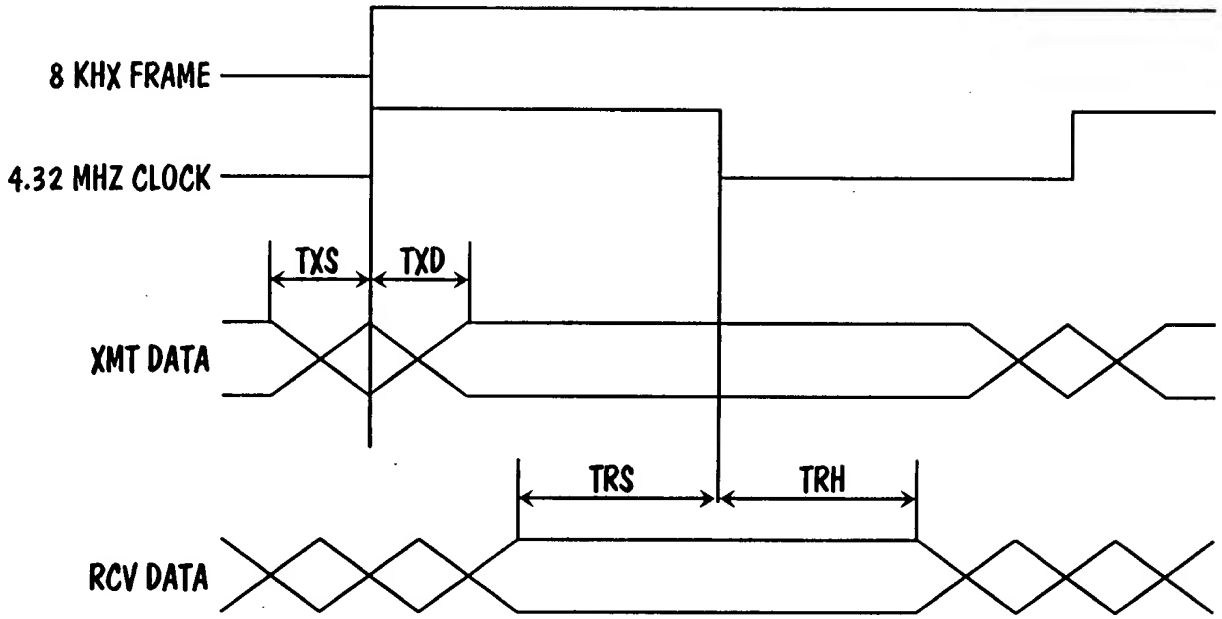

FIG. 20

PARAMETER	DESCRIPTION	MIN	MAX
TXS	TRANSMIT SKEW		30 NSEC
TXD	TRANSMIT DELAY		60 NSEC
TRS	RECEIVE SETUP	30 NSEC	
TRH	RECEIVE HOLD	60 NSEC	

FIG. 21

BYTE		POS.		POS.		POS.	
0	K1 PORT 1	1	K2 PORT 1	2	K1 PORT 2	3	K2 PORT 2
4	K1 PORT 3	5	K2 PORT 3	6	K1 PORT 4	7	K2 PORT 4
8	K1 PORT 5	9	K2 PORT 5	10	K1 PORT 6	11	K2 PORT 6
12	K1 PORT 7	13	K2 PORT 7	14	K1 PORT 8	15	K2 PORT 8
16	K1 PORT 9	17	K2 PORT 9	18	K1 PORT 10	19	K2 PORT 10
20	K1 PORT 11	21	K2 PORT 11	22	K1 PORT 12	23	K2 PORT 12
24	K1 PORT 13	25	K2 PORT 13	26	K1 PORT 14	27	K2 PORT 14
28	K1 PORT 15	29	K2 PORT 15	30	K1 PORT 16	31	K2 PORT 16
32	E1 PORT 1	33	F1 PORT 1	34	SPARE	35	SPARE
36	SPARE	37	SPARE	38	SPARE	39	SPARE
40	SPARE	41	SPARE	42	SPARE	43	SPARE
44	SPARE	45	SPARE	46	SPARE	47	SPARE
48	SPARE	49	SPARE	50	SPARE	51	SPARE
52	SPARE	53	SPARE	54	SPARE	55	SPARE
56	SPARE	57	SPARE	58	SPARE	59	SPARE
60	SPARE	61	SPARE	62	SPARE	63	SPARE

FIG. 22

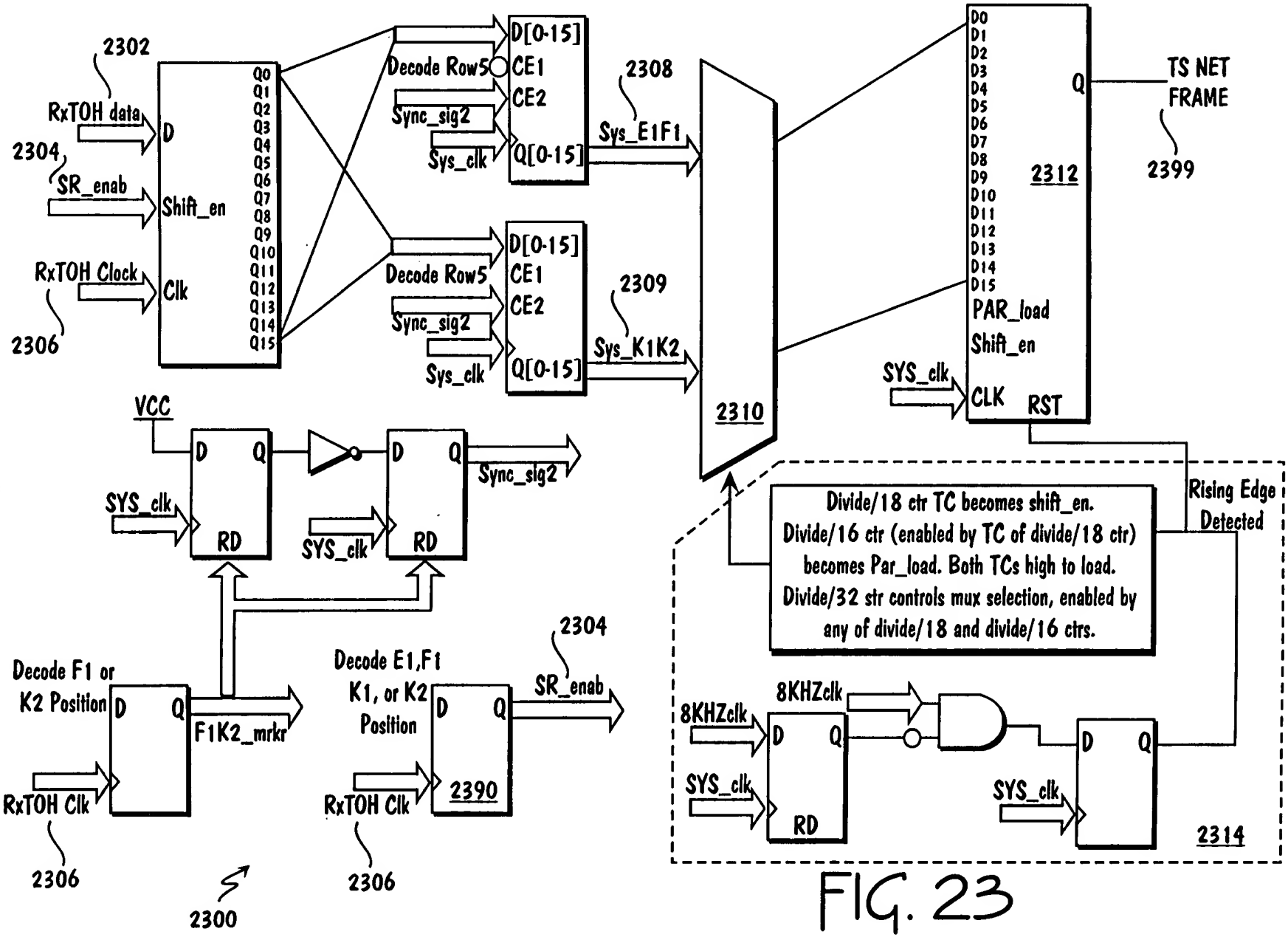
2302
RxTOH data
2304
SR_enab
Shift_en
RxTOH Clock
Clk
2306
D
Q0
Q1
Q2
Q3
Q4
Q5
Q6
Q7
Q8
Q9
Q10
Q11
Q12
Q13
Q14
Q15
Decode Row5
Sync_sig2
Sys_clk
D[0-15]
CE1
CE2
Q[0-15]
2308
Sys_E1F1
2309
Sys_K1K2
2310
D0
D1
D2
D3
D4
D5
D6
D7
D8
D9
D10
D11
D12
D13
D14
D15
PAR_load
Shift_en
CLK
RST
2312
Q
TS NET FRAME
2399
SYS_clk
VCC
D
Q
RD
Sync_sig2
Divide/18 ctr TC becomes shift_en.
Divide/16 ctr (enabled by TC of divide/18 ctr) becomes Par_load. Both TCs high to load.
Divide/32 str controls mux selection, enabled by any of divide/18 and divide/16 ctrs.
Rising Edge Detected
Decode F1 or K2 Position
F1K2_mrkr
Decode E1,F1 K1, or K2 Position
2390
8KHZclk
2314
2300

FIG. 23

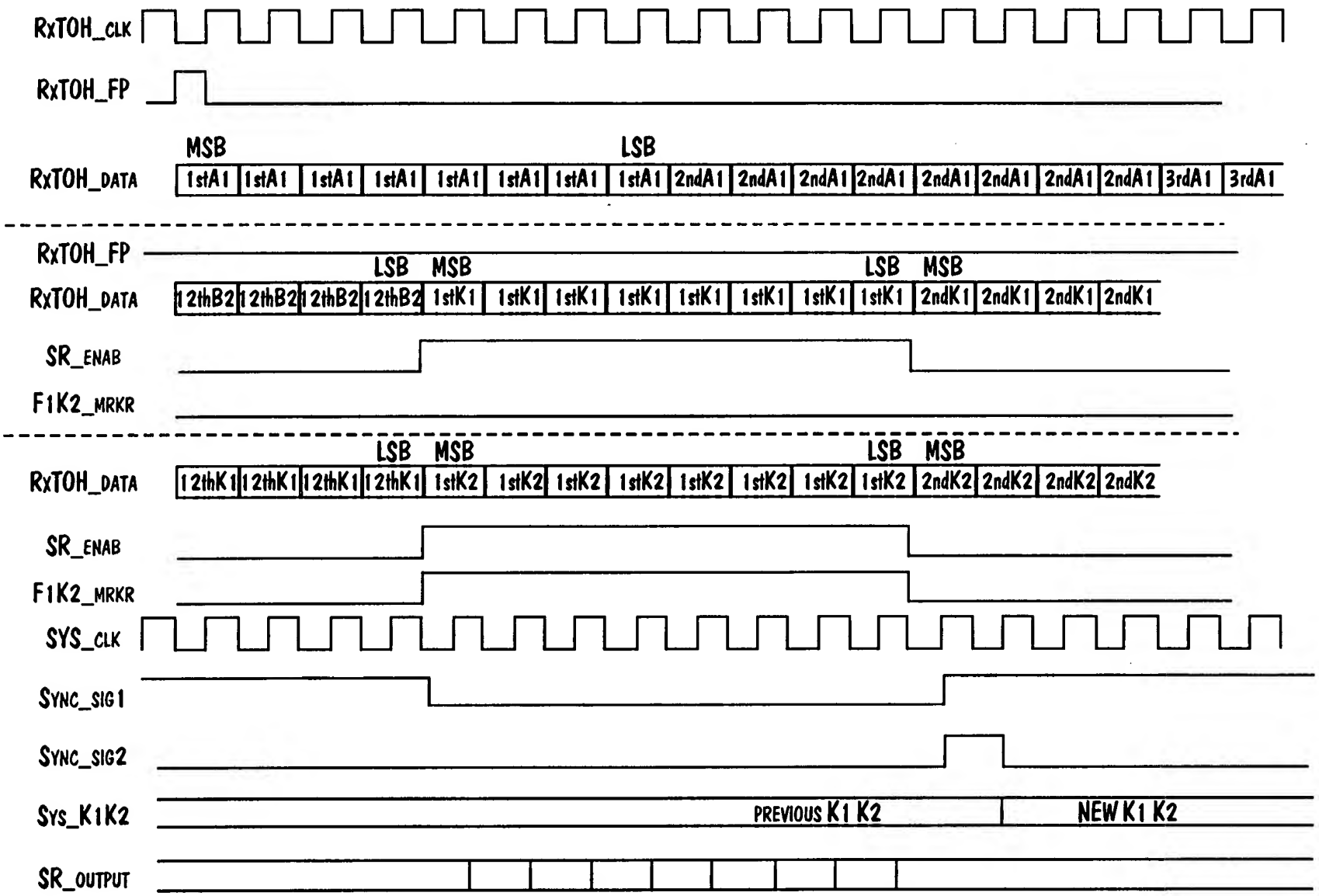
RxTOH_CLK
RxTOH_FP
MSB
LSB
RxTOH_DATA
1stA1 1stA1 1stA1 1stA1 1stA1 1stA1 1stA1 1stA1 2ndA1 2ndA1 2ndA1 2ndA1 2ndA1 2ndA1 2ndA1 2ndA1 3rdA1 3rdA1
RxTOH_FP
LSB MSB
LSB MSB
RxTOH_DATA
12thB2 12thB2 12thB2 12thB2 1stK1 1stK1 1stK1 1stK1 1stK1 1stK1 1stK1 1stK1 2ndK1 2ndK1 2ndK1 2ndK1
SR_ENAB
F1K2_MRKR
LSB MSB
LSB MSB
RxTOH_DATA
12thK1 12thK1 12thK1 12thK1 1stK2 1stK2 1stK2 1stK2 1stK2 1stK2 1stK2 1stK2 2ndK2 2ndK2 2ndK2 2ndK2
SR_ENAB
F1K2_MRKR
SYS_CLK
SYNC_SIG1
SYNC_SIG2
SYS_K1K2
PREVIOUS K1 K2
NEW K1 K2
SR_OUTPUT

FIG. 24

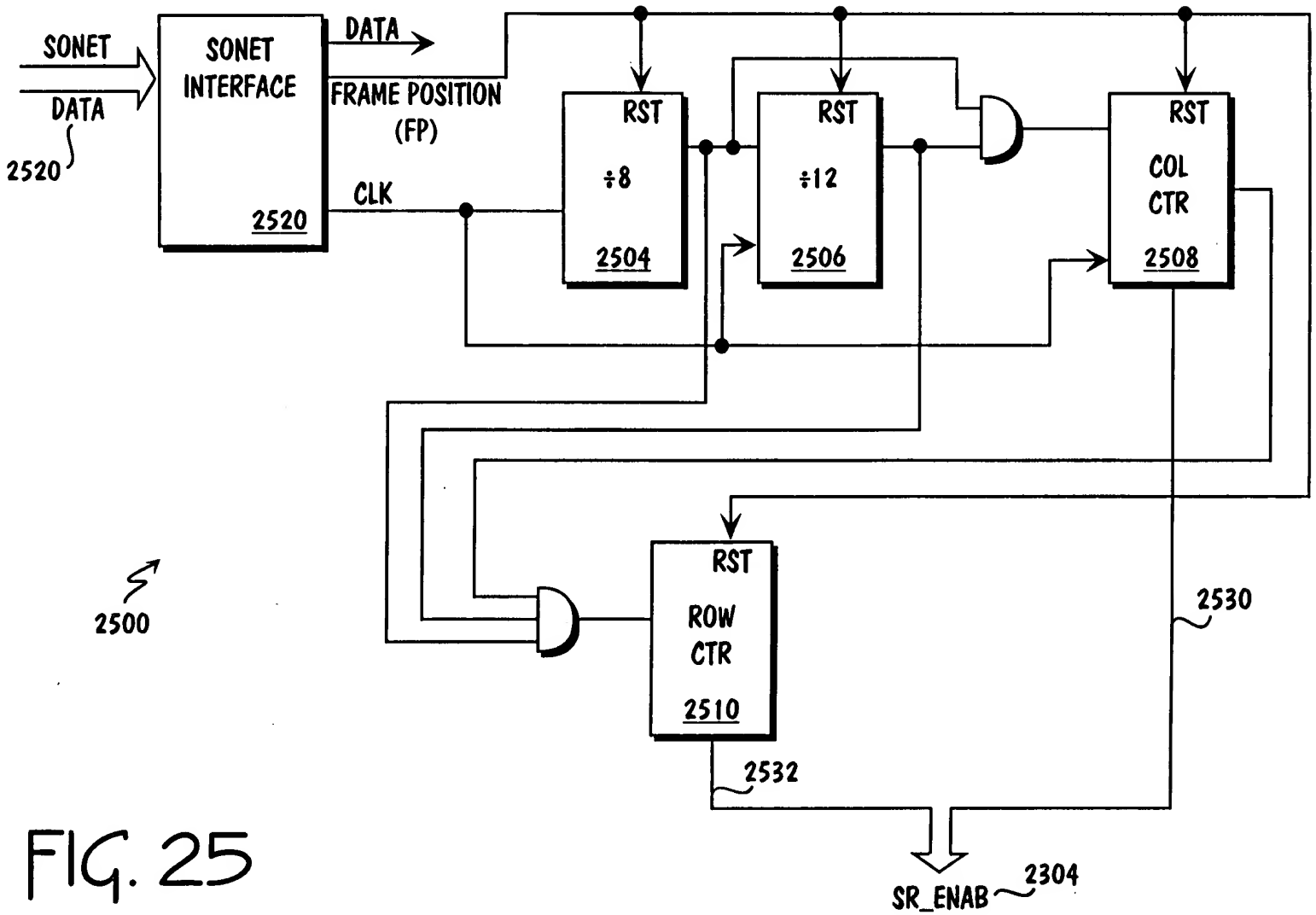
SONET
DATA
2520
SONET INTERFACE
2520
DATA
FRAME POSITION (FP)
CLK
RST
÷8
2504
RST
÷12
2506
RST
COL CTR
2508
RST
ROW CTR
2510
2500
2530
2532
SR_ENAB
2304

FIG. 25

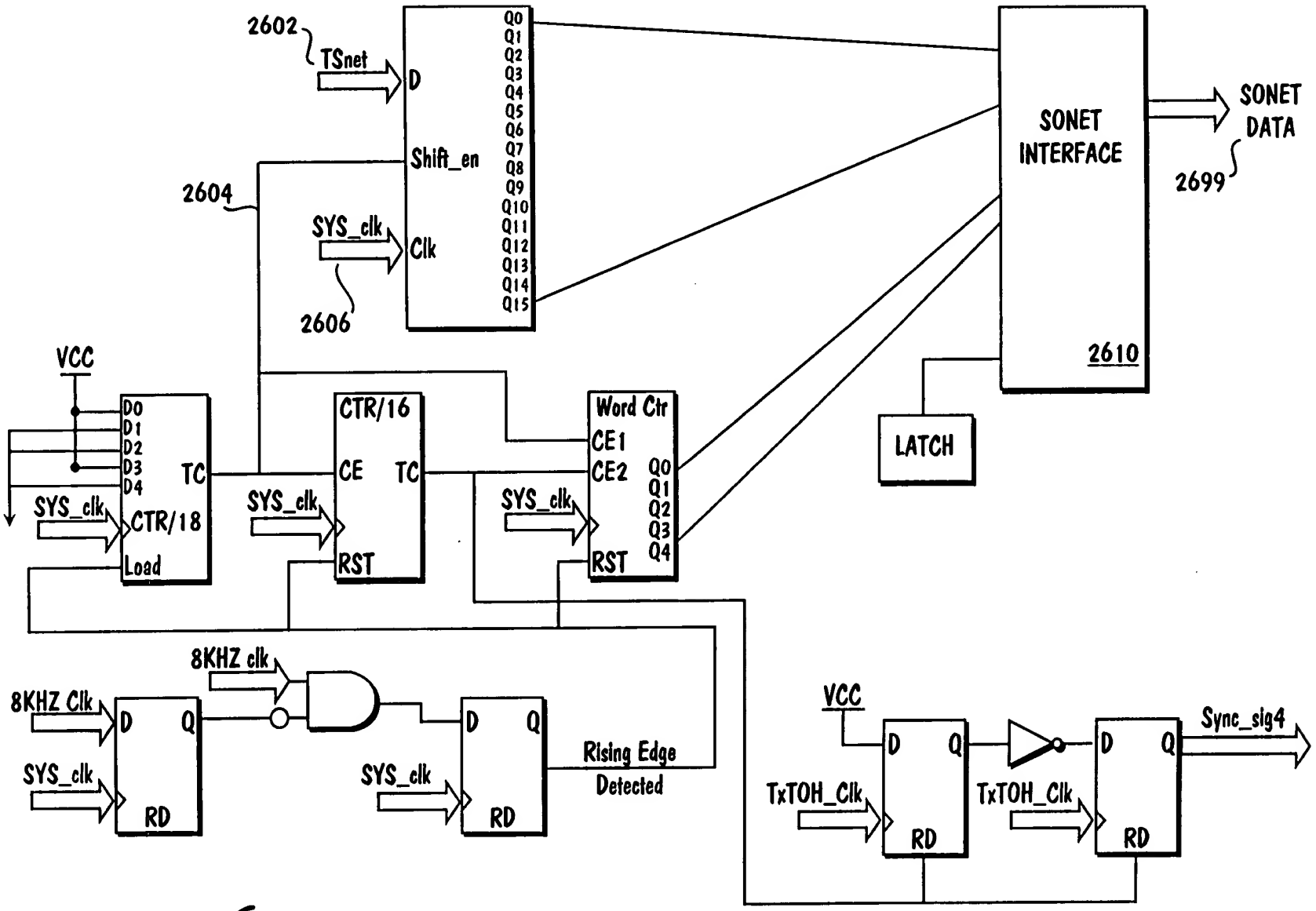
2602
TSnet
D
Shift_en
2604
SYS_clk
Clk
2606
Q0
Q1
Q2
Q3
Q4
Q5
Q6
Q7
Q8
Q9
Q10
Q11
Q12
Q13
Q14
Q15
SONET INTERFACE
2610
SONET DATA
2699
LATCH
VCC
D0
D1
D2
D3
D4
TC
SYS_clk
CTR/18
Load
CTR/16
CE
TC
SYS_clk
RST
Word Ctr
CE1
CE2
Q0
Q1
Q2
Q3
Q4
SYS_clk
RST
8KHZ clk
8KHZ Clk
D
Q
SYS_clk
RD
D
Q
SYS_clk
RD
Rising Edge Detected
VCC
D
Q
TxTOH_Clk
RD
D
Q
TxTOH_Clk
RD
Sync_sig4

FIG. 26

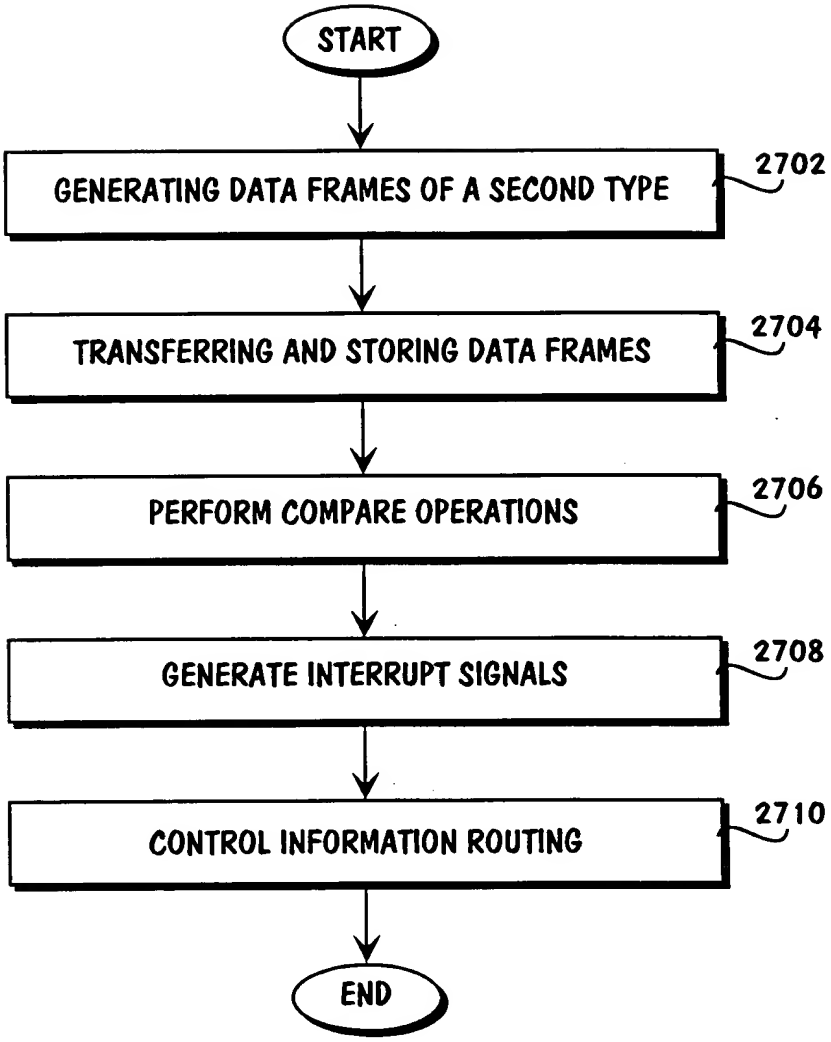

FIG. 27

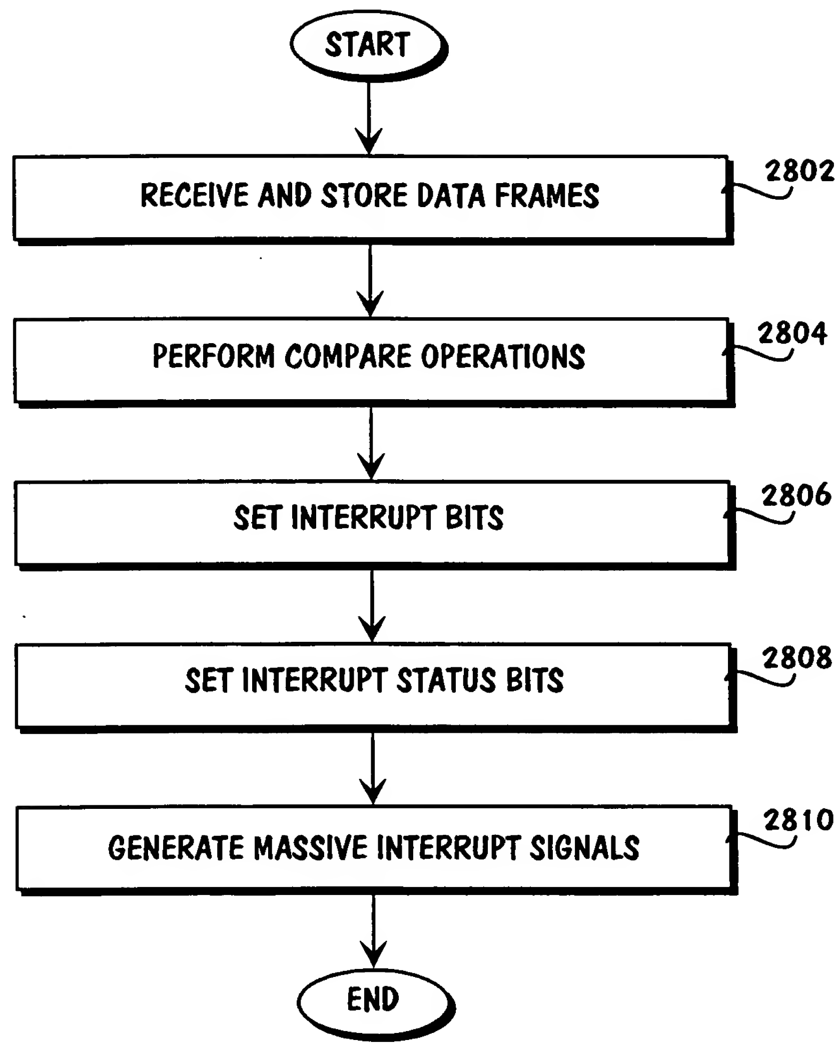
START
RECEIVE AND STORE DATA FRAMES
2802
PERFORM COMPARE OPERATIONS
2804
SET INTERRUPT BITS
2806
SET INTERRUPT STATUS BITS
2808
GENERATE MASSIVE INTERRUPT SIGNALS
2810
END

FIG. 28

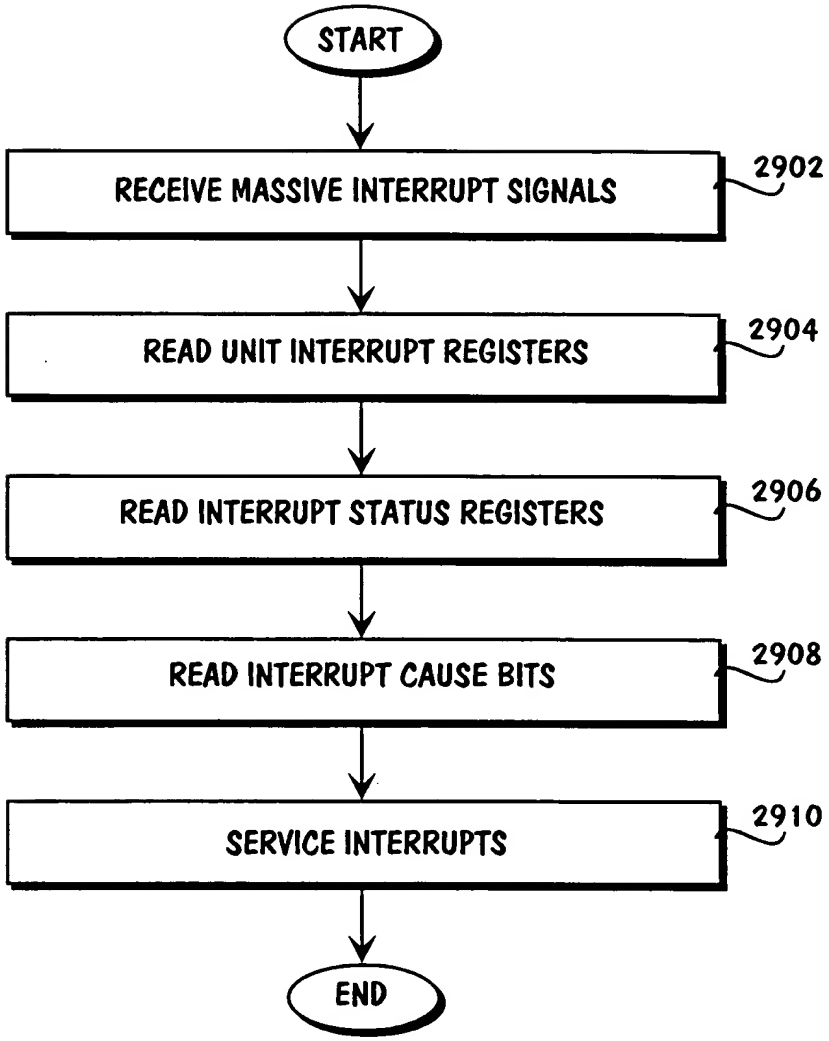
START
RECEIVE MASSIVE INTERRUPT SIGNALS
2902
READ UNIT INTERRUPT REGISTERS
2904
READ INTERRUPT STATUS REGISTERS
2906
READ INTERRUPT CAUSE BITS
2908
SERVICE INTERRUPTS
2910
END

FIG. 29